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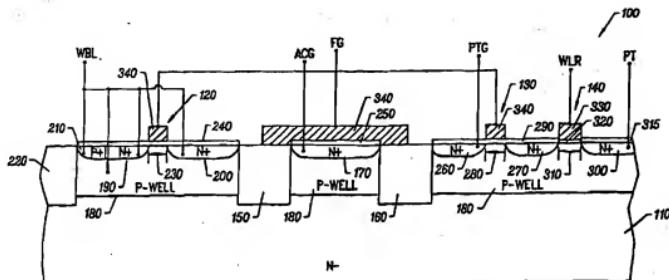
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(71) Applicant: LATTICE SEMICONDUCTOR CORPORATION [US/US]; 995 Stewart Drive, Sunnyvale, CA 94088 (US).		Published <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>	
(72) Inventors: MEHTA, Sunil, D.; 1004 Oaktree Drive, San Jose, CA 95129 (US). LI, Xiao-Yu; 4060 Bouquet Park, San Jose, CA 95135 (US).			
(74) Agents: FLIESLER, Martin, C. et al.; Fliesler Dubb Meyer and Lovejoy LLP, Suite 400, Four Embarcadero Center, San Francisco, CA 94111-4156 (US).			

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(54) Title: EEPROM CELL USING P-WELL FOR TUNNELING ACROSS A CHANNEL



(57) Abstract

An EEPROM cell is described that is programmed and erased by electron tunneling across an entire portion of separate transistor channels. The EEPROM cell has three transistors formed in a P-well of a semiconductor substrate. The three transistors are a tunneling transistor (NMOS), a sense transistor (NMOS) and a read transistor (NMOS). Electron tunneling occurs to program the EEPROM cell through a sense tunnel oxide layer upon incurrence of a sufficient voltage potential between a floating gate and the sense channel. Electron tunneling also occurs to erase the EEPROM cell through a tunnel oxide layer upon incurrence of a sufficient voltage potential between the floating gate and the tunneling channel.

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**EEPROM CELL USING P-WELL FOR
TUNNELING ACROSS A CHANNEL****BACKGROUND OF THE INVENTION****Field of the Invention**

This invention relates generally to semiconductor devices, and more particularly, to an electrically erasable programmable read only memory ("EEPROM") cell.

Description of Related Art

The semiconductor community faces increasingly difficult challenges as it moves into production of semiconductor devices at feature sizes approaching 0.1 micron. Cell designs for typical semiconductor devices must be made more reliable, scalable, cost effective to manufacture and able to operate at lower power in order for manufacturers to compete in the semiconductor industry. EEPROM devices are one of such semiconductor devices that must meet these challenges.

EEPROM devices are generally known as read-only memory in which the memory cells that store information may be erased and reprogrammed electrically. An EEPROM cell is typically made up of three separate transistors, namely, a write transistor, a sense transistor and a read transistor. The EEPROM cell is able to be programmed, erased and read by removing or adding electrons to a floating gate. Thus, for example, the floating gate may be programmed by removing free electrons from the floating gate and thereby giving the floating gate a positive charge. When it is desired to erase an EEPROM cell, the floating gate is given a net negative charge by injecting electrons onto the floating gate. The read operation is performed by reading the state (current) of the sense transistor. In order to give the floating gate a positive charge (program) or negative charge (erase), electron tunneling, for example using the well-known Fowler-Nordheim tunneling technique, may be performed by applying the appropriate voltage potentials between the floating gate and a region, such as a drain region, of a transistor. Upon applying the appropriate voltage potentials, electron tunneling occurs through a tunnel oxide layer between the floating gate and the region.

As the feature sizes of EEPROM cells are scaled downward, the prior art EEPROM cells exhibit certain scalability, cost and reliability limitations. First, the manufacturing process for a smaller EEPROM cell becomes more complex and, accordingly, manufacturing costs rise as transistor channel lengths are reduced. For example, as the channel length of a transistor of the EEPROM cell is scaled downward, the thickness of the gate oxide overlying

5 the channel must also be reduced since the gate oxide thickness must be scaled with the
channel length. In view of the fact that EEPROM cells already have a complex process to
form multiple oxide thicknesses, additional oxide thicknesses for the transistors would add
additional steps to further complicate the manufacturing process and thereby increase
manufacturing costs.

10 In addition to this scaling problem, reliability problems also exist with previous
EEPROM cells. First, the EEPROM cell is typically both programmed and erased through
the same small tunnel oxide window at the edge of a transistor region that may deteriorate the
cell quickly. In general, the tunnel oxide window deteriorates after tens of thousands of
program/erase cycles and that deterioration cycle is shortened by only using the small tunnel
oxide window for both programming and erasing operations. Thus, in addition to the size of
the tunnel oxide window, the use of the window for both programming and erasing of the
15 EEPROM cell causes the cell to be significantly less reliable. A further reliability limitation
of previous EEPROM cells is that the tunnel oxide window is often less reliable because it is
formed over a highly doped program junction (PRJ). The high doping concentration of the
PRJ degrades the oxide immediately above the PRJ and thereby reduces the EEPROM cell's
20 reliability. A still further limitation of the EEPROM cell is that the voltages needed to
program, erase and read the cell are high due to the relatively large feature sizes of the cell.
Thus, in order to achieve lower voltages to operate the EEPROM cell, feature sizes of the cell
must be scaled downward.

25 Thus, a need exists for a redesigned EEPROM cell that (1) does not add costly steps
to the manufacturing process, (2) does not suffer from reliability problems caused by
programming and erasing through the edge of a small tunnel oxide window, (3) does not
deteriorate through use of a PRJ oxide and (4) operates at a lower power by using smaller
feature sizes.

30 **SUMMARY OF THE INVENTION**

An EEPROM cell is described that is programmed and erased by electron tunneling
across an entire portion of separate transistor channels, rather than at an edge of a transistor
region, by using a P conductivity type well. The EEPROM cell has three transistors formed
in a semiconductor substrate: a tunneling transistor, a sense transistor and a read transistor.
35 The tunneling transistor has a tunneling source, a tunneling drain, and a tunneling channel
between the tunneling source and the tunneling drain. The tunneling transistor, the sense

5 transistor and the read transistor are formed in a well that has a P conductivity type that is opposite the N conductivity type of the semiconductor substrate. The tunneling source and the tunneling drain have the N conductivity type. A tunnel oxide layer is formed over the tunneling channel, the tunnel source and the tunnel drain. Between the tunneling transistor and the sense transistor is a program junction region, also formed in the well of the semiconductor substrate, and separated from the tunneling transistor by a first oxide and separated from the sense transistor by a second oxide. The program junction region, having an N conductivity type, also has a program junction oxide layer overlying the program junction region. The sense transistor is also formed in the well in the semiconductor substrate. The sense transistor has a sense source, sense drain and a sense channel between the sense source and the sense drain where both the sense source and the sense drain have an N conductivity type. A sense tunnel oxide layer overlies the sense channel, the sense source and the sense drain. The read transistor, also formed in the well in the semiconductor substrate, is electrically connected to the sense transistor through the sense drain. A floating gate overlies the tunnel oxide layer, the program junction oxide layer and the sense tunnel oxide layer. Electron tunneling through the tunnel oxide layer overlying the tunnel channel occurs upon incurrence of a sufficient voltage potential between the floating gate and the tunneling channel. Electron tunneling through the sense tunnel oxide layer overlying the sense channel occurs upon incurrence of a sufficient voltage potential between the floating gate and the sense channel.

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The EEPROM cell of the present invention further provides electron tunneling through the tunnel oxide layer overlying the tunneling channel to occur across the entire portion of the tunneling channel instead of only across an edge of a region as in previous EEPROM cells. Likewise, the EEPROM cell of the present invention provides electron tunneling through the sense tunnel oxide layer overlying the sense channel to occur across the entire portion of the sense channel. The EEPROM cell of the present invention further allows erasing only across the tunneling channel and programming only across the sense channel to thereby separate the program and erase operations. The EEPROM cell further has reduced thicknesses for the tunnel oxide layer, the program junction oxide layer, the sense tunnel oxide layer and the read gate oxide layer to improve scalability and reduce operating voltages of the EEPROM cell of the present invention.

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BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention can be obtained when the following detailed description of a preferred embodiment is considered in conjunction with the following drawings, in which:

FIG. 1 is a cross-sectional view of an embodiment of the EEPROM cell of the present invention; and

FIG. 2 is a circuit diagram view of an embodiment of the EEPROM cell of the present invention.

It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the drawings have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to other elements for purposes of clarity. Further, where considered appropriate, reference numerals have been repeated among the drawings to represent corresponding or analogous elements.

DETAILED DESCRIPTION

Alternative embodiments of the structure of the EEPROM cell of the present invention are described below, along with the general process for manufacturing those embodiments. The operation of those embodiments is then provided in Table 1 and described in detail to explain the programming, erasing and reading functions of the EEPROM cell embodiments of the present invention.

FIG. 1 is a cross-sectional view of an embodiment of the EEPROM cell of the present invention. In FIG. 1, the embodiment of the EEPROM cell 100 is formed on a semiconductor substrate 110, for example a silicon substrate, and has an N conductivity type. In one embodiment, the semiconductor substrate is a bulk substrate being entirely formed of an N conductivity type material. In another embodiment, the semiconductor substrate is formed of a N conductivity type material having an epitaxial layer on a top surface where the epitaxial layer is formed of an N conductivity type material. The P and N conductivity type materials (known as dopants) are those materials commonly known in the art that alter the conductivity of a semiconductor material by contributing either a hole (P type) or an electron (N type) to the conduction process. For silicon substrates, the dopants are generally found in Groups III and V of the well-known chemical periodic table. In alternative embodiments, the semiconductor substrate 110 may be alternative silicon materials well-known in the semiconductor industry such as germanium, germanium/silicon, gallium arsenide, polysilicon,

5 silicon on insulator or the like. The EEPROM cell 100 has three separate transistors formed
in the semiconductor substrate 110, namely, a tunneling transistor 120, a sense transistor 130
and a read transistor 140. A program junction region 170 is also formed in the semiconductor
substrate 110 and is electrically separated from the tunneling transistor 120 by a first oxide
150, e.g. silicon dioxide, also formed in the semiconductor substrate 110. The program
10 junction region 170 has an N conductivity type, such as an N+ conductivity type, and is a
highly doped N+ region. A second oxide 160 is used to separate the sense transistor 130 from
the program junction region 170. The second 160 oxide, like the first oxide 150 and oxide
region 220, is composed of an insulating material, such as silicon dioxide. Returning to the
tunneling transistor 120, the tunneling transistor 120 has a tunneling source 190 and a
15 tunneling drain 200, all formed within a well 180. A P+ region 210, having a P conductivity
type, is formed in the substrate 110 using conventional implant techniques in order to provide
electrical connection between the Word Bit Line to the well 180. The well 180 has a P
conductivity type and is therefore a P-well 180. In contrast, the tunneling source 190 and
tunneling drain 200 have the N conductivity type. The tunneling transistor 120 is therefore
20 a NMOS transistor in this embodiment. By using a NMOS transistor in a P-well 180, the
entire tunneling channel 230 may be used to perform electron tunneling that has certain
benefits as described below. This is because the well 180, in addition to the tunneling source
190 and tunneling drain 200, may be electrically connected together to create the appropriate
potential across the entire tunneling channel 230 to allow the entire tunneling channel 230
25 to be used for electron tunneling. The sense transistor 130, read transistor 140 and the
program junction region 170 are also formed in the well 180. A tunneling channel 230 is
formed in well 180 between the tunneling source 190 and tunneling drain 200. Overlying the
tunneling source 190, the tunneling channel 230 and the tunneling drain 200 is a tunnel oxide
layer 240. The tunnel oxide layer 240 is typically composed of an insulating material, such
30 as silicon dioxide, and has a thickness in the range of approximately 70 to 90 angstroms, and
in one embodiment, is approximately 80 angstroms. It is noted that such a thickness for the
tunnel oxide layer 240 is considerably less than the approximate 150 angstroms or greater
used in prior art devices which improves the EEPROM cell 100 scaleability. Overlying the
program junction region 170 is a program junction oxide layer 250 that is composed of an
insulating material, such as silicon dioxide. The program junction oxide layer 250 has a
35 thickness in the range of approximately 80 to 105 angstroms, and in one embodiment, is
approximately 96 angstroms, which is also an improvement over prior art devices that had

5 thicknesses greater than 180 angstroms. It is noted that while the thickness of the tunnel
oxide layer 240 is approximately 80 angstroms and the thickness of the program junction
oxide layer is 96 angstroms, both layers may be deposited or grown (using conventional oxide
deposition techniques) in a single process step. This is because the program junction oxide
layer 250 is grown on a highly doped N⁺ program junction region 170 that characteristically,
10 as is well known to one skilled in the art, "expands" the thickness of the program junction
oxide layer 250 to 96 angstroms, while the tunnel oxide layer 240, overlying the N type
tunneling source 190 and the N type tunneling drain 200, remains at 80 angstroms. Thus,
additional process steps, to form oxide layers with different thicknesses, are avoided.

15 Returning to FIG. 1, the sense transistor 130 has a sense source 260 and a sense drain
270 formed in the semiconductor substrate 110. A sense channel 280 is formed between the
sense source 260 and the sense drain 270 in the well 180. The conductivity of the sense
source 260 and the sense drain 270 is of an N type. Overlying the sense source 260, the sense
drain 270 and the sense channel is a sense tunnel oxide layer 290 having an approximate
20 thickness of 80 angstroms. As earlier described, the sense tunnel oxide layer 290 may also
be simultaneously formed with the tunnel oxide layer 240 and the program junction oxide
layer 250. Depending on the mode of sense transistor 140 (depletion or enhancement mode),
the relevant voltages for operating the EEPROM cell 100 are adjusted. The sense transistor
130 is, in one embodiment, a depletion mode transistor, as is commonly understood in the
industry. In a further embodiment, the sense transistor 130 is an enhancement mode
25 transistor (also is also commonly known in the industry).

30 The read transistor 140 shares the sense drain 270 with the sense transistor 130
which acts as the read source 270. The read transistor 140 also has a read drain 300 that has
an N conductivity type. Overlying the read drain 300 is a read drain oxide 315 layer that is
composed of an insulating material, such as silicon dioxide, and has an approximate thickness
of 80 angstroms. The read drain oxide layer 315 is formed in the same step as the tunnel
oxide layer 240, the program junction oxide layer 250 and the sense tunnel oxide layer 290.
Between the read source 270 and the read drain 300 is a read channel 310 in the well 180.
Overlying the read channel 310 is a read gate oxide layer 320 that has a thickness of
approximately 35 angstroms and is composed of an insulating material, such as silicon
dioxide. The formation of the read gate oxide layer 320 requires additional separate process
35 steps than the oxide layers 240, 250, 290 and 315 since the thickness of the read gate oxide
layer 320 is considerably less than the others. A read gate 330 overlies the read gate oxide

5 layer 320 and is composed of a conducting material, such as a polycrystalline silicon material. A floating gate 340 overlies the tunnel oxide layer 240 overlying the tunneling channel 230 of the tunneling transistor 120, the program junction oxide layer 250 and the sense tunnel oxide layer 290 overlying the sense channel 280 of the sense transistor 130. The floating gate 340 is also formed of a conducting material, such as a polycrystalline silicon material.

10 The transistors 120, 130, 140 of the EEPROM cell 100 are electrically connected to certain electrical lines and gates in order to operate and control the functions of the EEPROM cell 100. As shown in FIG. 1, a Word Bit Line (WBL) is electrically connected to the well 180, tunneling source 190 and tunneling drain 200. WBL is further electrically connected to the P+ region 210 to provide electrical contact from the WBL to the well 180. The WBL is electrically connected to the tunneling transistor 120 (tunneling source 190, tunneling drain 200 and P-well 180) so that the entire portion of the tunneling channel 230 may be used to 15 erase the EEPROM cell 100 as described below. An Array Control Gate (ACG) is electrically connected to the program junction region 170 while a Product Term Ground (PTG) is electrically connected to the sense source 260 of the sense transistor 130. A Word Line Read (WLR) is electrically connected to the read gate 330 of the read transistor 140 and a Product 20 Term (PT) is electrically connected to the read drain 300. It is understood that electrical connecting includes any manner of transmitting charge between the two items being connected.

25 The method of manufacturing the EEPROM cell 100 of FIG. 1 includes standard deposition and etching techniques for forming the EEPROM cell 100 shown in FIG. 1. For example, in one embodiment, the EEPROM cell 100 is formed as follows. The semiconductor substrate 110, which may have an epitaxial layer (not shown) on the top surface of the semiconductor substrate 110, is patterned and etched (using conventional techniques) to form deep trenches in the semiconductor substrate 110 for the oxide regions 220, 150, and 160 of 30 FIG. 1. The well 180 is then formed by implanting the appropriate conductivity type into the semiconductor substrate 110. The tunnel oxide layer 240, the program junction oxide layer 250, the sense tunnel oxide layer 290 and the read oxide layer 315 are then formed using common deposition or oxide growing techniques. In one embodiment, these layers are formed as follows. An oxide layer is grown across the entire semiconductor substrate having an 35 approximate thickness of about 50 to 60 angstroms. Using conventional patterning techniques, the oxide layer is masked except for the area overlying the read channel 310. Etching is then performed to remove the oxide layer overlying the read channel 310. A

5 second oxide layer having a thickness of approximately 35 angstroms is then formed over the oxide layer and the semiconductor surface overlying the read channel 310. At this point, a 35 angstrom oxide layer (read gate oxide layer 320) has been formed. Also, the other oxide layers (tunnel oxide layer 240, program junction oxide layer 250, sense tunnel oxide layer 290) have also been formed, each having a combined thickness of approximately 80 angstroms
 10 (approximately 50 angstrom oxide layer and 35 angstrom second oxide layer). The thickness of these oxides is therefore approximately 80 angstroms, except for the program junction oxide layer 250 that is approximately 96 angstroms. After these oxide layers have been formed, the gates 340,330 for the transistors 120,130,140, including the floating gate 340, are formed and patterned using conventional techniques. The gates are typically formed of a conducting material, e.g. a polycrystalline silicon material. Next, the source and drain implants are formed for each transistor 120, 130, 140 and standard back end (as is commonly known to those skilled in the art) is performed. It is understood that a plurality of EEPROM cells are manufactured into an EEPROM device in order to store a multitude of information. The EEPROM cell further includes numerous metallization layers (not shown) overlying the cell
 15 20 100 to electrically connect the cell 100 to other cells and other devices in an EEPROM device, as well as passivation layers (not shown) to protect the cell 100.

The three operations of the EEPROM cell 100 are program, erase and read. The various voltages applied to the EEPROM cell to perform these operations are shown in Table 1 below.

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TABLE 1

	<u>WBL</u>	<u>ACG</u>	<u>PTG</u>	<u>WLR</u>	<u>PT</u>
Program	HiZ	V_{pp}	ground	V_{ee}	ground
Erase	V_{pp}	ground	ground or HiZ	ground	HiZ
Read (Depletion Mode)	HiZ	ground	ground	V_{ee}	$V_{ee}/2 (V_t)$
Read (Enhancement Mode)	HiZ	V_{ee}	ground	V_{ee}	$V_{ee}/2 (V_t)$

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The program operation of the EEPROM cell 100 of FIG. 1 is defined, for this embodiment, as providing a net negative charge on the floating gate 340. For the erase operation, a positive charge is provided on the floating gate 340. It is understood, however, that alternative embodiments may deviate from this definition, yet fall within the scope of the

5 present invention as claimed below. That is, the erase operation may put a negative charge on the floating gate 340 as long as the program operation puts the opposite charge (positive) on the erase operation. Thus, alternative embodiments may create potentials between the floating gate 340 and the appropriate channels that provide a net negative charge on the floating gate 340 to erase the EEPROM cell 100 of FIG. 1 and provide a positive charge on the floating gate 340 to program the EEPROM cell 100. Again, the erase operation is merely the consistent opposite of the program operation. In a further embodiment, the difference in charge level may differentiate between a program and erase operation. Thus, by increasing a charge to a sufficient level, the operation may change from a program operation to an erase operation, or vice versa.

10 In order to program the EEPROM cell 100 of FIG. 1, in one embodiment, the floating gate 340 is given a negative charge by moving electrons to the floating gate 340. The method of moving electrons to the floating gate 340 is commonly known to those skilled in the art as Fowler-Nordheim tunneling. In general, this process has electrons tunnel through a barrier, for example a thin oxide layer, in the presence of a high electric field. However, unlike previous EEPROM cells that performed the electron tunneling through a small oxide window at the edge of a source or drain region, the present invention provides for electron tunneling across a transistor channel. Further, the entire portion of the channel is used for electron tunneling rather than only an edge of a region as has been previously done since a NMOS transistor in a P-well is used for the tunneling transistor 120. The advantages of such electron tunneling are described below.

15 In one embodiment, programming of the EEPROM cell 100 of FIG. 1 is performed by moving electrons to the floating gate 340 through the sense tunnel oxide layer 290 and across the entire portion of the sense channel 280. It is understood that the entire portion of the sense channel 280 means the distance between the sense source 260 and the sense drain 270 underlying the sense tunnel oxide layer 290. In order to move the electrons to floating gate 340 to program the EEPROM cell 100, V_{pp} , for example 10 volts, is applied to ACG. Since the program junction region 170 is capacitively coupled to the floating gate 340 through the program junction oxide layer 250, approximately 8 volts is placed on the floating gate 340. WBL is placed at a floating voltage of HiZ, that is, WBL is not connected to a voltage or ground and therefore has a varying potential. 20 PTG and PT are grounded while WLR is set to V_{ss} , for example 1.8 volts. Since the floating gate 340 is at a high voltage and the sense source 260 is grounded (through channel formation since the read transistor is on) as well as the substrate 110, a potential is created between the floating gate 25

5 340 and the sense channel 280. The sense tunnel oxide layer 290 immediately above the sense channel 280 has a thickness of approximately 80 angstroms, in one embodiment, so that electron tunneling occurs across the entire portion of the sense channel 280 and through the sense tunnel oxide layer 290 since the programming voltages previously mentioned provide a sufficient voltage potential between the floating gate 340 and the sense channel 280. The voltages provided in this embodiment may vary in alternative embodiments as long as a sufficient potential is created to move electrons through the sense tunnel oxide layer 290 onto the floating gate 340 across the sense channel 280. Likewise, the oxide layer thicknesses, of all oxide layers used for electron tunneling, may also vary as long as the thickness is sufficient to permit electron tunneling at the disclosed potentials.

10 To erase the floating gate 340, in this same embodiment, electrons are removed from the floating gate 340 through the tunnel oxide layer 240 across the entire portion of the tunnel channel 230 to give the floating gate 340 a positive charge. To erase the EEPROM cell 100, V_{pp} , for example 10 volts, is applied to WBL while ACG, PTG, and WLR are all grounded. In another embodiment, PTG is provided a HiZ voltage. PT is provided a HiZ voltage. Since the tunneling source 190, tunneling drain 200 and the well 180 are at a relatively high voltage (10 volts) while the floating gate 340 is at a low voltage, a potential is created between the floating gate 340 across the entire portion of the tunnel channel 230 so that an electrons tunnel through the tunnel oxide layer 240 from the floating gate 340 across the entire portion of the tunnel channel 230. The erasing operation, in this embodiment, is done in bulk (multiple cells are erased at one time), while the programming operation is selective to certain cells.

15 The EEPROM cell 100 has numerous advantages over previous EEPROM cells. First, the channels 280 and 230 are used to program and erase, respectively, the EEPROM cell. The electron tunneling is therefore performed through a transistor channel rather than a source/drain region. By using an NMOS transistor in a P-well 180 for the tunneling transistor 120, the entire tunneling channel 230 may be used to perform electron tunneling. This is because the well 180, in addition to the tunneling source 190 and tunneling drain 200, may be electrically connected together to allow the entire tunneling channel 230 to be used for electron tunneling. By tunneling across a channel, the reliability of the EEPROM cell is increased since a larger oxide, rather than a small oxide window, is used for programing and erasing operations. Further, the entire channel is used to program and erase as opposed to the edge of a source/drain region. By using the entire channel, reliability of the EEPROM device increases since the entire oxide layer is used rather than only an edge of an oxide layer. Still further, the reliability of the EEPROM device of FIG. 1 increases over

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5 prior art devices since the erase and program functions are performed over separate regions, tunnel channel 230 and sense channel 280, rather than the same tunneling window as previously used to perform both program and erase operations. The EEPROM cell of FIG. 1 further has the advantage of having thinner oxide layers 240, 250, 290, and 310 which decreases the cell size. Prior art devices had oxide layer thicknesses in excess of 150 angstroms while the present oxide layers have
10 angstroms in the range of 35 to 96 angstroms. Additionally, the present EEPROM cell 100 does not perform the electron tunneling through the PRJ and therefore the tunnel oxide quality is not degraded which provides better cell data retention. Furthermore, the scaling of the tunnel oxide regions from 96 to 80 angstroms means that V_{pp} may also be scaled down which provides an EEPROM cell that operates at lower power.

15 The EEPROM cell 100 of FIG. 1 is read by determining the state of sense transistor 130. In one embodiment, the sense transistor 130 is a depletion mode transistor in which WBL is set to a HiZ, ACG and PTG are grounded, WLR is set to V_{ce} , for example 1.8 volts, and PT is set to V_t ($V_{ce}/2$), for example 0.7 volts. If the sense transistor 130 is an enhancement mode transistor, ACG is set to V_{ce} , for example 1.8 volts, while the remaining voltages remain the same. Thus, the state
20 of sense transistor 140 is a logical 1 during erase since a positive charge is on floating gate 340 while a logical 0 is the state of sense transistor 140 during program. The sense transistor 140 reads a logical 1 if current flows from sense source 260 to sense drain 270. If no current flows, a logical 0 results.

25 FIG. 2 is a circuit diagram view of the embodiment of the EEPROM cell of FIG. 1. In FIG. 2, the three transistors of FIG. 1 including the tunneling transistor 120, the sense transistor 130, and the read transistor 140 are shown. Likewise, the tunneling transistor 120 is shown to be electrically connected to WBL, while the sense source 260 is electrically connected to PTG and ACG is capacitively coupled through the tunnel oxide layer 250 to the floating gate 340.

30 The EEPROM cell of the present invention has been described in connection with the embodiments disclosed herein. Although an embodiment of the present invention has been shown and described in detail, along with variances thereof, many other varied embodiments that incorporate the teachings of the invention may be easily constructed by those skilled in the art that may fall within the scope of the present invention as claimed below.

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CLAIMS

What is claimed is:

1. An EEPROM cell, comprising:
 - a semiconductor substrate, said semiconductor substrate having an N conductivity type;
 - a well formed in said semiconductor substrate, said well having a P conductivity type;
 - 10 a tunneling transistor formed in said well, said tunneling transistor having a tunneling source, a tunneling drain and a tunneling channel between said tunneling source and said tunneling drain, said tunneling drain and said tunneling source having said N conductivity type;
 - a tunnel oxide layer overlying said tunneling channel, said tunneling source and said tunneling drain;
 - 15 a program junction region formed in said well, said program junction region separated from said tunneling transistor by a first oxide, said program junction region having said N conductivity type;
 - a program junction oxide layer overlying said program junction region;
 - 20 a sense transistor formed in said well and separated from said program junction region by a second oxide, said sense transistor having a sense source, a sense drain and a sense channel between said sense source and said sense drain, said sense source and said sense drain having said N conductivity type;
 - a sense tunnel oxide layer overlying said sense channel, said sense source and said sense drain;
 - 25 a read transistor formed in said well, said read transistor electrically connected to said sense transistor through said sense drain; and
 - a floating gate overlying said tunnel oxide layer, said program junction oxide layer and said sense tunnel oxide layer.
2. The EEPROM cell of claim 1, wherein electron tunneling through said tunnel oxide layer overlying said tunneling channel occurs upon incurrence of a sufficient voltage potential between said floating gate and said tunneling channel, and wherein electron tunneling through said sense tunnel oxide layer overlying said sense channel occurs upon incurrence of a sufficient voltage potential between said floating gate and said sense channel.

5 3. The EEPROM cell of claim 2, wherein said electron tunneling through said tunnel oxide layer overlying said tunneling channel occurs across an entire portion of said tunneling channel.

10 4. The EEPROM cell of claim 2, wherein said electron tunneling through said sense tunnel oxide layer overlying said sense channel occurs across an entire portion of said sense channel.

5. The EEPROM cell of claim 2, wherein said electron tunneling through said tunnel oxide layer only erases said EEPROM cell.

6. The EEPROM cell of claim 2, wherein said electron tunneling through said sense tunnel oxide layer only programs said EEPROM cell.

15 7. The EEPROM cell of claim 2, further comprising:
a word bit line (WBL) electrically connected to said tunneling source, said tunneling drain and said well;
an array control gate (ACG) electrically connected to said program junction region;
a product term ground (PTG) electrically connected to said sense source;
20 a product term (PT) electrically connected to a read drain of said read transistor; and
a word line read (WLR) electrically connected to said read transistor, wherein said WBL, ACG, PTG, PT and WLR provide said sufficient voltage potential between said floating gate and said tunneling channel and said sufficient voltage potential between said floating gate and said sense channel.

25 8. The EEPROM cell of claim 7, wherein said sufficient voltage potential between said floating gate and said sense channel is accomplished by providing a floating voltage to said WBL, approximately 10 volts to said ACG, approximately 0 volts to said PTG and said PT, and approximately 1.8 volts to said WLR.

30 9. The EEPROM cell of claim 7, wherein said sufficient voltage potential between said floating gate and said tunneling channel is accomplished by providing approximately 10 volts to said WBL, approximately 0 volts to said ACG, said PTG and said WLR, and

5 a floating voltage to said PT.

10. The EEPROM cell of claim 7, wherein said sufficient voltage potential between said floating gate and said tunneling channel is accomplished by providing approximately 10 volts to said WBL, approximately 0 volts to said ACG and said WLR, and a floating voltage to said PTG and said PT.

10 11. The EEPROM cell of claim 7, wherein said sufficient voltage potential between said floating gate and said tunneling channel is accomplished by providing approximately 10 volts to said WBL, approximately 0 volts to said ACG, said PTG and said WLR, and a floating voltage to said PT.

15 12. The EEPROM cell of claim 11, wherein said sense transistor is a depletion mode transistor.

13. The EEPROM cell of claim 7, wherein a current flows between said sense source and said sense drain when said WBL has a floating voltage, said ACG and said PTG has approximately 0 volts, said WLR has approximately 1.8 volts and said PT has approximately 0.7 volts.

20 14. The EEPROM cell of claim 13, wherein said sense transistor is an enhancement mode transistor.

15. The EEPROM cell of claim 1, wherein said tunnel oxide layer has a thickness of approximately 80 angstroms.

25 16. The EEPROM cell of claim 1, wherein said program junction oxide layer has a thickness of approximately 96 angstroms.

17. The EEPROM cell of claim 1, wherein said sense tunnel oxide layer has a thickness of approximately 80 angstroms.

5 18. An EEPROM cell, comprising:
a semiconductor substrate, said semiconductor substrate having an N conductivity type;
a well formed in said semiconductor substrate, said well having a P conductivity type;
a tunneling transistor formed in said well, said tunneling transistor having a tunneling
source, a tunneling drain and a tunneling channel between said tunneling
source and said tunneling drain, said tunneling drain and said tunneling source
having said N conductivity type, said tunneling source, tunneling drain, and
well being electrically connected to a word bit line;
a tunnel oxide layer overlying said tunneling channel, said tunneling source and said
tunneling drain;
15 a program junction region formed in said well, said program junction region separated
from said tunneling transistor by a first oxide, said program junction region
having said N conductivity type, said program junction region being electrically
connected to an array control gate;
a program junction oxide layer overlying said program junction region;
20 a sense transistor formed in said well and separated from said program junction region
by a second oxide, said sense transistor having a sense source, a sense drain
and a sense channel between said sense source and said sense drain, said sense
source and said sense drain having said N conductivity type, said sense source
being electrically connected to a product term ground;
25 a sense tunnel oxide layer overlying said sense channel, said sense source and said sense
drain;
a read transistor formed in said well, said read transistor electrically connected to said
sense transistor through said sense drain, said read transistor having a read
source, a read drain, and a read channel between said read source and said read
drain, said read drain having an N conductivity type and being electrically
connected to a product term;
30 a read gate oxide layer overlying said read channel; and
a floating gate overlying said tunnel oxide layer, said program junction oxide layer and
said sense tunnel oxide layer, wherein electron tunneling through said tunnel
oxide layer overlying said tunneling channel occurs upon incurrence of a
sufficient voltage potential between said floating gate and said tunneling
channel, and wherein electron tunneling through said sense tunnel oxide layer

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overlying said sense channel occurs upon incurrence of a sufficient voltage potential between said floating gate and said sense channel.

19. The EEPROM cell of claim 18, wherein said read gate oxide layer has a thickness of approximately 35 angstroms.

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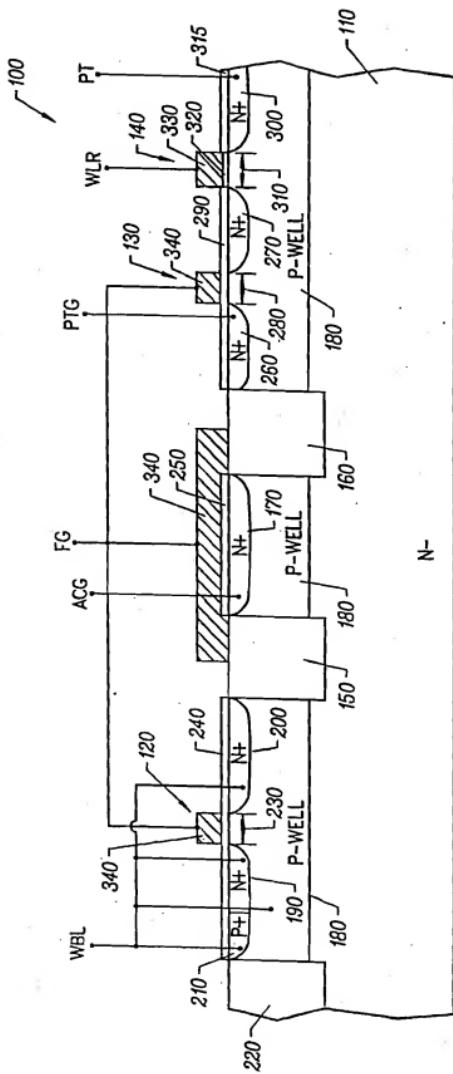


FIG. 1

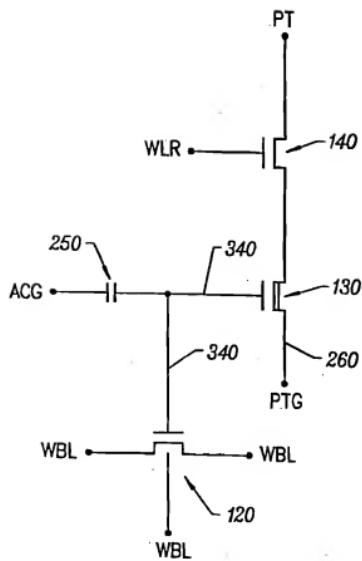


FIG. 2

INTERNATIONAL SEARCH REPORT

Int'l. Search Application No

PCT/US 99/29916

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 HO1L27/115 G11C16/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 HO1L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 5 646 901 A (SHARPE-GEISLER BRADLEY A ET AL) 8 July 1997 (1997-07-08) the whole document	1-19
A	US 5 504 706 A (D ARRIGO IANO ET AL) 2 April 1996 (1996-04-02) the whole document	1-19
A	US 5 615 150 A (BARSAN RADU ET AL) 25 March 1997 (1997-03-25) the whole document	1-19
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Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

Int'l. Jpn. Application No.
PCT/US 99/29916

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Information on patent family members

Int'l. Jonal Application No

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